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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/707,388
Filing Date: December 10, 2003
Appellant(s): DIVAKARUNI ET AL.

Carl F. Ruoff
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 8, 2008 appealing from the Office action mailed April 11, 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner: the rejection of claims 12-18 and 20 under 35 U.S.C § 112, second paragraph has been withdrawn.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,168,984 Yoo et al. 01-2001

Wolf, "Silicon Processing for the VLSI Era: Process Integration," Vol. II, 1990, pp. 146, 176, 193.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Insofar as definite, claims 12, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoo et at. '984.

The limitation of "a silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers" found in product claims 12 and 20 invokes the product-by-process doctrine. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps (*MPEP § 2113*). Therefore, anticipation of claims 12 and 20 does not require the silicide section to be formed by silicidation, only that the material used for the silicide has a known silicidation temperature which meets the requirements of the claim.

By both the conventional definition in the art and by the Applicant's definition provided in the specification, a back-end-of-line (BEOL) layer can comprise any ILD layer (Applicant's specification, ¶16, "ILD layer may be any BEOL layer…containing a via and/or metal.") or any metal layer (Applicant's specification, ¶18, "conventional BEOL wiring structure could be…a via to underlying wiring layers or a simple wire."), so

long as the layer is formed over the front-end-of-line (FEOL) structures found on a silicon substrate.

Yoo discloses a semiconductor device comprising: a silicide resistor (fig. 13; layer 30c is formed of polysilicon layer 30a and tungsten silicide layer 30b; col. 8, lines 54-66; layers 30a/30b have an inherent resistance, thus considered a resistor) in one of a plurality of back-end-of-line layers (formed in interlayer dielectric 27 formed over FEOL layers 1-17; layer 31 is a second BEOL layer, thus 27 and 31 are a plurality), the silicide resistor including a silicide section (30b, tungsten silicide) having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers (tungsten silicide inherently has a silicidation temperature of ~600ºC) and a polysilicon base (30a) positioned below the silicide section; wherein the silicide section and the polysilicon base are is positioned in a trough in one of the plurality of BEOL layers (layers 30a/30b formed in trough opening of layer 27; col. 8, lines 36-53).

Wolf, Vol. II (NPL Reference "U", previously provided) provides further evidence of the inherency of the silicidation temperature of tungsten (group VIII) metals being ~600 °C (p. 146). This silicidation temperature of tungsten is read as "a silicidation temperature less than a damaging temperature of the plurality of BEOL layers" in light of the fact that the Applicant's specification gives illustrative examples (species) of silicidation temperatures less than a damaging temperature of the plurality of BEOL layers (genus) that includes 600 °C for tungsten silicide. Yoo discloses the plurality of BEOL layers to comprise silicon oxide, which is well known in the art to be able to withstand temperatures of ~ 600°C without damage.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo et al. '984 in view of Wolf, Vol. II (NPL Reference "U", previously provided).

Yoo discloses all of the elements of the claims as discussed in paragraph 4, including the use of tungsten silicide, but the references does not explicitly teach the use of cobalt silicide, palladium silicide, platinum silicide or nickel silicide.

Wolf teaches the use of group VIII silicides, including cobalt, palladium, platinum, and nickel silicide, in BEOL resistors (Wolf defines "multilevel interconnects" to include ILD layers, vias, and metal lines (p. 176), thereby meaning BEOL layers as defined above; and because interconnects inherently have a resistance, they are classified as "resistors"). Wolf also teaches the inherent resistivity associated with each silicide (p. 193, Table 4.3; p. 146): cobalt silicide has a resistivity between 14-20 μ-ohm/cm (p. 193, Table 4.3); palladium silicide has a resistivity between 25-30 μ-ohm/cm (p. 146); platinum silicide has a resistivity between 26-35 μ-ohm/cm (p. 193, Table 4.3); and nickel silicide has a resistivity of 50 ohm/cm (p. 146). Wolf teaches the silicidation temperature of the group VIII metals as 600 °C or less (p. 146), which reads on a silicidation temperature less than a damaging temperature of the plurality of BEOL layers as defined above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the cobalt silicide, palladium silicide, platinum silicide or nickel silicide material of Wolf in the resistor of Yoo. One would have been motivated to do this because Wolf taught that tungsten, cobalt, palladium, platinum and nickel were art recognized functional equivalents for forming silicides in semiconductor devices (p. 146) (MPEP § 2144.06).

(10) Response to Argument

Regarding the Appellant's arguments for the rejection of claims 12-18 and 20 under 35 U.S.C § 112, second paragraph:

a) The Appellant's arguments with respect to the rejection of claims 12-18 and 20 under 35 U.S.C § 112, second paragraph have been fully considered and are persuasive. Therefore, the rejection of claims 12-18 and 20 under 35 U.S.C § 112, second paragraph has been withdrawn.

Regarding the Appellant's arguments for the rejection of claims 12, 18 and 20 under 35 U.S.C § 102(b) as anticipated by Yoo et al. (US 6,168,984):

a) The Appellant asserts that the opening in layer 27 (Fig. 12) of Yoo which contains interconnect element 30a/30c is not a trough because it extends though layer 27, which allows contact to element 25. Appellant asserts that "A trough is defined as a channel. The opening in Yoo is not a channel because as it extends through layer 27." (Appellant's Brief, page 5, lines 3-4). This argument is not found

persuasive because Yoo teaches the formation of interconnect element 30a/30c to comprise a damascene process (col. 8, lines 54-55). It is well known in the art that a damascene process is defined as forming a trench in a dielectric layer to create an interconnect pattern, filling the patterned trench with metal, and polishing the metal down to the surface of the dielectric to form the metal interconnect. This process is precisely what Yoo performs, and therefore the trench formed in dielectric layer 27 is equivalent to the claimed trough, regardless of whether a contact hole is also formed in the damascene trench. The process of forming a contact hole along with the trench is well known in the art as a “dual damascene” process, and is described by Yoo in col. 8, lines 48-52. Simply because Yoo forms a contact within layer 27 and below interconnect 30c does not negate the existence of the trough formed for interconnect line 30a/30c. As such, Appellant’s arguments that Yoo does not teach a trough are not persuasive.

b) The Appellant asserts that a “bitline is not a resistor and a bitline positioned in an opening that connects each side of insulating layer 27 is not a resistor positioned in a tough. A bitline is an electrical connection." (Appellant's Brief, page 5, lines 6-7). The Examiner asserts that a resistor is well known in the art to also be an electrical connection, and therefore by Appellant’s definition a bitline can be a resistor. Further, claims 12, 18 and 20 do not require the polysilicon and silicide material of the resistor to comprise a specific resistivity, therefore the fact that the polysilicon and tungsten silicide bitline 30a/30c of Yoo has a given resistivity, as is well known in the art and evidenced by the Wolf reference (Table 4.3, p. 193), defines 30a/30c

as a resistor. As such, Appellant's arguments that Yoo does not teach a resistor in a trough are not persuasive

Regarding the Appellant's arguments for the rejection of claims 13-17 under 35 U.S.C § 103(a) over Yoo et al. (US 6,168,984) in view of Wolf ("Silicon Processing for the VLSI Era: Process Integration," Vol. II, 1990, pp. 146, 176, 193):

a) The Appellant's arguments are similar to those presented for claims 12, 18 and 20, in that Yoo does not teach a resistor in a trough, and therefore those arguments are not perusasive for the reasons stated hereinabove. Further, Appellant asserts that "Wolf only discloses using silicides for interconnect applications, not for a resistor application as claimed in the current invention." (Appellant's Brief, page 5, lines 4-6 of Section 3). As stated above, an interconnect has a specific resistivity, and can therefore be considered a resistor in the context of the claims. Specifically, the claimed resistivities of the silicides of claims 13-17 are within the typical resistivity range used for silicide interconnects, as taught by Wolf on pages 146 and 193. As such, Appellant's arguments that Yoo in view of Wolf does not teach the claimed resistor in a trough are not persuasive

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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